CLAIMS

The invention claimed is:

1. An interface circuit for processing an analog color signal comprising:

a phase locked loop (PLL) circuit adapted to generate a plurality of phased signals from a synchronizing signal that is associated with the color signal;

a phase adjuster adapted to generate a delay signal from two of the phased signals that are apart from each other by an odd multiple of approximately 45 degrees; and

an analog to digital converter adapted to process the color signal as controlled by the delay signal.

2. The circuit of claim 1, wherein

the synchronizing signal is intended to generate a pixel clock in a display, and

the phased signals replicate those of the pixel clock.

3. The circuit of claim 1, wherein

the phase adjuster includes:

a first phase selector for selecting a first one of the phased signals;

a second phase selector for selecting a second one of the phased signals; and

a phase mixer for multiplying the first selected phased signal with a first weight, multiplying the second selected phased signal with a second weight, and adding together the first and the second multiplied phased signals to derive the delay signal.

4. The circuit of claim 3, wherein

the phase adjuster further includes:

a decoder to generate phase selection signals for selecting the first and second phased signals.

5. The circuit of claim 4, wherein

some of the phase selection signals are received into the phase mixer.

6. The circuit of claim 3, wherein

the phase adjuster further includes:

a Phase Digital to Analog Converter for generating a first weight signal representing the first weight and a second weight signal representing the second weight, and

wherein the phase mixer receives the first weight signal and the second weight signal to derive the delay signal.

7. The circuit of claim 6, wherein

the phase adjuster further includes:

a decoder to generate weight selection signals for generating the first and second weight signals.

8. The circuit of claim 6, wherein

the first and second weights have a substantially constant sum total weight.

9. The circuit of claim 8, wherein

the Phase Digital to Analog converter includes

a first current source drawing a first current that represents the first weight,

a second current source drawing a second current that represents the sum total weight, and

a third current source drawing a difference current between the second current and the first current, wherein the difference current is used to derive the second weight signal.

10. The circuit of claim 8, wherein

the sum total weight equals a multiplication integer times four, and

the first weight equals the multiplication integer times one of zero, one, two, three and four.

11. A device comprising:

means for deriving a plurality of phased signals from a synchronizing signal associated with the color signal;

means for deriving the delay signal from two of the phased signals that are apart from each other by an odd multiple of approximately 45 degrees; and

means for using the delay signal to control conversion of the color signal into digital form.

12. The device of claim 11, wherein

the means for deriving the phased signals includes phase locked loop (PLL) circuit.

13. A method for generating a delay signal for processing an analog color signal, comprising:

deriving a plurality of phased signals from a synchronizing signal associated with the color signal;

deriving the delay signal from two of the phased signals that are apart from each other by an odd multiple of approximately 45 degrees; and

using the delay signal to control conversion of the color signal into digital form.

14. The method of claim 13, wherein

the phased signals are derived in a phase locked loop (PLL) circuit.

15. The method of claim 14, wherein

the synchronizing signal is intended to generate a pixel clock in a display, and

the four phased signals replicate those of the pixel clock.

16. The method of claim 13, wherein

deriving is performed by:

determining the location of a general requested delay in a phase diagram; and

selecting the two phased signals such that they define a sector between on the phase diagram that encompasses the general required delay.

17. The method of claim 16, further comprising:

multiplying a first one of the selected phased signals with a first preselected weight,

multiplying a second one of the selected phased signals with a second preselected weight, and

adding together the first and the second multiplied phased signals.

18. The method of claim 17, further comprising:

selecting first and second weights so as to simulate the general requested delay within the sector.

19. The method of claim 18, further comprising:

subtracting the first weight from a preset sum total weight to derive the second weight.

20. The method of claim 19, wherein

the sum total weight equals a multiplication integer times four, and

the first weight equals the multiplication integer times one of zero, one, two, three and four.